Notice of Allowability	Application No.	Applicant(s)	
	10/811,351	SON ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 2/24/2006*.

2. ☒ The allowed claim(s) is/are *9-16*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Amendment

1. Applicant's explanation of the instant invention with the amendment in pointing the difference with the cited prior art was found to be persuasive.

Allowable Subject Matter

2. Claims 9 – 16 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Claim 9 recites, inter alia, a method of forming a ferroelectric memory device comprising the steps of polishing an insulating laver on a plurality of ferroelectric capacitors with a silica slurry to reduce the height of the insulating layer above a surface of the plurality of ferroelectric capacitors so that the surface remains covered by a portion of the insulating laver, polishing the insulating layer further with a ceria slurry to further reduce the height of the insulating laver and to expose a polishing stop laver on the surface of the plurality of ferroelectric capacitors wherein polishing an insulating layer on a plurality of ferroelectric capacitors with a silica slurry is preceded by forming a mask that covers the insulating layer on a peripheral circuit region of the ferroelectric memory device and exposes the insulating layer on a cell array region of the ferroelectric memory device and etching-back the insulating layer on the cell array region to a height that is less than a height of the insulating layer on peripheral circuit region, the method further comprising the steps of polishing the insulating layer on the plurality of ferroelectric capacitors with the silica slurry to reduce the height of the insulating layer on the cell array region, removing the mask from the insulating layer on

the peripheral circuit region and polishing the insulating layer on the cell array region and on the peripheral circuit region with the ceria slurry to expose the polishing stop layer and to reduce a step difference between respective height of the insulating layer on the cell array region and on the peripheral circuit region. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 10 – 16 recite, inter alia, a method of manufacturing a ferroelectric memory device, the method comprising the steps of forming a plurality of ferroelectric capacitors in a cell array region on a substrate, forming a barrier layer to cover ferroelectric capacitors in the cell array region and on the peripheral circuit region, forming a polishing stop layer on the cell array region and on the peripheral circuit region to cover the barrier layer, forming an insulating layer on the cell array region and on the peripheral circuit region to cover the polishing stop layer, removing a portion of the insulating layer only in the cell array region to provide a first insulating pattern having a height above a surface ferroelectric capacitors in the cell array region, planarizing the first insulating pattern in the cell array region and the peripheral circuit region using chemical mechanical polishing to form a planarized second insulating pattern that exposes the polishing stop layer; and removing the exposed portion of the polishing stop layer and the barrier layer disposed thereunder until the top surface of the ferroelectric capacitor is exposed. The art of record does not disclose or anticipate the

above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Conclusion

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Homma, US 2002/0068452 teaches cerium oxide slurries for polishing fragile dielectric layers..

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
March 16, 2006

Primary Examiner